REMARKS

This responds to the Office Action mailed on August 24, 2005. No claims are amended, canceled or added herein. Claims 1-100 remain pending in this application. Of these pending claims, claims 80-100 currently stand withdrawn.

§103 Rejection of the Claims

Claims 54-71 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Han (U.S. 6,611,452) in view of Coe (U.S. 4,754,310). Applicant respectfully traverses, and submits that a prima facie case supporting a §103 rejection has not been provided for at least the following reasons.

The rejection relies on Coe as disclosing "a high voltage semiconductor device where in Fig. 1, the intrinsic region made up of alternating layers 11 and 12 is situated between anode and cathode 21 and 23." Applicant disagrees, noting that region 11 is identified as being a first conductivity type (e.g. n-type), and region 12 is identified as being a second conductivity type (e.g. p-type). Col. 7 lines 41-45. Thus, the suggested combination of references would not provide, among other things, an NDR diode with an intrinsic region (e.g. an NDR p/i/n diode or an NDR n/i/p diode). Additionally, Applicant respectfully asserts that the rejection has not provided objective evidence suggesting the desirability of combining Han and Coe. Applicant respectfully submits that "to have a memory cell with higher performance" is conclusory, and does not provide objective evidence identifying why the addition of alternating layers 11 and 12 of Coe to the device of Han would provide the higher performance, nor does it provide objective evidence that otherwise fairly indicates a suggestion to combine the alternating layers 11 and 12 of Coe to the device of Han.

With respect to independent claim 54, Applicant is unable to find, among other things, in the cited portions of the Han and Coe references a showing or fair suggestion of a memory cell with a Negative Differential Resistance (NDR) p/i/n diode including a p-type anode, an n-type cathode, and an intrinsic region positioned between the anode and the cathode, as recited in the claim. With respect to independent claim 63, Applicant is unable to find, among other things, in the cited portions of the Han and Coe references a showing or fair suggestion of a memory cell with a Negative Differential Resistance (NDR) n/i/p diode including an n-type anode, a p-type

cathode, and an intrinsic region positioned between the anode and the cathode. Claims 55-62 depend on claim 51 and are believed to be in condition for allowance at least for the reasons provided with respect to claim 54. Claims 64-71 depend on claim 63 and are believed to be in condition for allowance at least for the reasons provided with respect to claim 63.

Applicant respectfully requests withdrawal of the rejection, and reconsideration and allowance of the claims.

Allowable Subject Matter

Claims 1-53 and 72-79 were allowed.

Withdrawn Claim 80-100

37 CFR §1.141(b) provides:

> Where claims to all three categories, product, process of making, and process of use, are included in a national application, a three way requirement for restriction can only be made where the process of making is distinct from the product. If the process of making and the product are not distinct, the process of using may be joined with the claims directed to the product and the process of making the product even though a showing of distinctness between the product and process of using the product can be made.

In the response dated March 19, 2004, Applicant asserted that claim 1 was a linking claim in so far as it is a claim to a product linking a process of making and a use (MPEP 809.03). Allowed claim 1 recites a memory cell, withdrawn claim 85 recites a method for forming a memory cell, withdrawn claim 84 recites a method for operating a memory cell. Applicant respectfully submits that a distinction has not been shown or asserted for the process recited in claim 85 and the product recited in claim 1. Thus, pursuant to §1.141(b) and in view of allowed claim 1, Applicant respectfully requests consideration and allowance of claim 80-100.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance, and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 373-6960 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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By his Representatives,

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Date 11-18-05

By _____
Marvin L. Beekman
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop Amendment, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 18 day of November, 2005.

KACIA LEE
Name

Kacia Lee
Signature